PRO-LOG®
CORPORATION

STD 7000

7614
TTL Input/Output Card

USER'S MANUAL

A Pro-Log OPENWARE™ Product

11/85

FOREWORD

This manual explains how to use Pro-Log's 7614 TTL Input/Output Card. It is structured to reflect the answers to basic questions that you might ask about the 7614. We welcome your suggestions on how we can improve our instructions.

The 7614 is an OPENWARE product in the Pro-Log Series 7000 STD BUS hardware. Our products are modular and provide industrial managers with the means of using their own people to control the design, production, and maintenance of products that use STD BUS hardware. Pro-Log also offers applications seminars based on STD BUS products.

OPENWARE, a trademark of Pro-Log Corporation, means our products are designed to quality standards with readily available, second-sourced, industry standard components, clear and complete specifications, full documentation, and the option to purchase the manufacturing rights and drawings.

You may also find the *STD BUS Technical Manual* useful in your work. If you would like a copy of this document, please write to us on your company letterhead.

Contents

	Page
Foreword	ii
Figures	iii
References & Bibliography	iv
Section 1. Specifications	1-1
Purpose	1-1
Features	1-1
Functional Description	1-2
Specifications	1-3
General	1-3
Electrical	1-3
Mechanical	1-5
Section 2. Installation	2-1
Introduction	2-1
Installation	2-1
Card Layout and Jumpers	2-2
Selecting a Mode	2-3
I/O Mapped Card Addressing	2-5
Eight-Bit Port Addressing	2-5
I/O Expansion	2-5
Ten-Bit Port Addressing	2-7
Section 3. Operation and Programming	3-1
Operation	3-1
Section 4. Operating Software	4-1
Section 5. Maintenance	5-1
Refrence Drawings	5-1
Return for Repair/Warranty	5-5

Figures

Figure		Page
1-1	7614 TTL Input/Output Card	1-1
1-2	Block Diagram	1-2
1-3	Read Timing	1-4
1-4	Write Timing	1-4
1-5	STD Edge Connector	1-5
1-6	User Interface Connector J1	1-5
1-7	User Interface Connector J2	1-5
1-8	User Interface Connector J3	1-5
1-9	User Interface Connector J4	1-6
1-10	Compatible Mating Connectors	1-6
2-1	Installation	2-1
2-2	Physical Layout and Jumper Options	2-2
2-3	Available Functions	2-3
2-4	Configuring for a Function	2-4
2-5	8-Bit I/O Address Selection (Mode 1)	2-5
2-6	8-Bit I/O Address Selection (Mode 2-4)	2-7
2-7	10-Bit I/O Address Selection (Mode 1)	2-8
2-8	10-Bit I/O Address Selection (Mode 2-4)	2-12
3-1	Typical 7614 I/O Circuit	3-1
5-1	Schematic	5-2
5-2	Assembly Drawing	5-3

REFERENCES/BIBLIOGRAPHY

STD Series 7000 Specification and Practice, Pro-Log Document #111684.
Series 7000 STD BUS Technical Manual, Pro-Log Document #107855.
Microprocessor User's Guide, Pro-Log Document #101145.

Section 1
SPECIFICATIONS

PURPOSE

The 7614 provides eight 8-bit TTL I/O ports, 64 I/O lines total. Each 8-bit port can be configured as an input, output,or output with readback.

The I/O lines are noninverting and the outputs can drive 16 LSTTL loads. The card can decode eight or ten address lines and the STD BUS I/O Expansion (IOEXP) line. Slip-on connectors allow mapping to any consecutive group of I/O addresses.

The I/O lines of the 7614 card are accessible at four 34-pin user interface connectors. The connectors are latching and allow for strain-relieved mating plugs to ensure a reliable mechanical connection.

FEATURES

- Eight 8-bit I/O ports, 64 lines
- Each port can be configured as an input, output, or output with readback
- Latching user interface connectors
- Can occupy four or eight I/O addresses
- Flexible I/O mapping
- Single +5V operation
- Processor independent
- 8- or 10-bit I/O port address decoding
- Supports I/O expansion bit
- Functionally compatible with Pro-Log 7601A, 7602A 7603A, and 7604A I/O cards

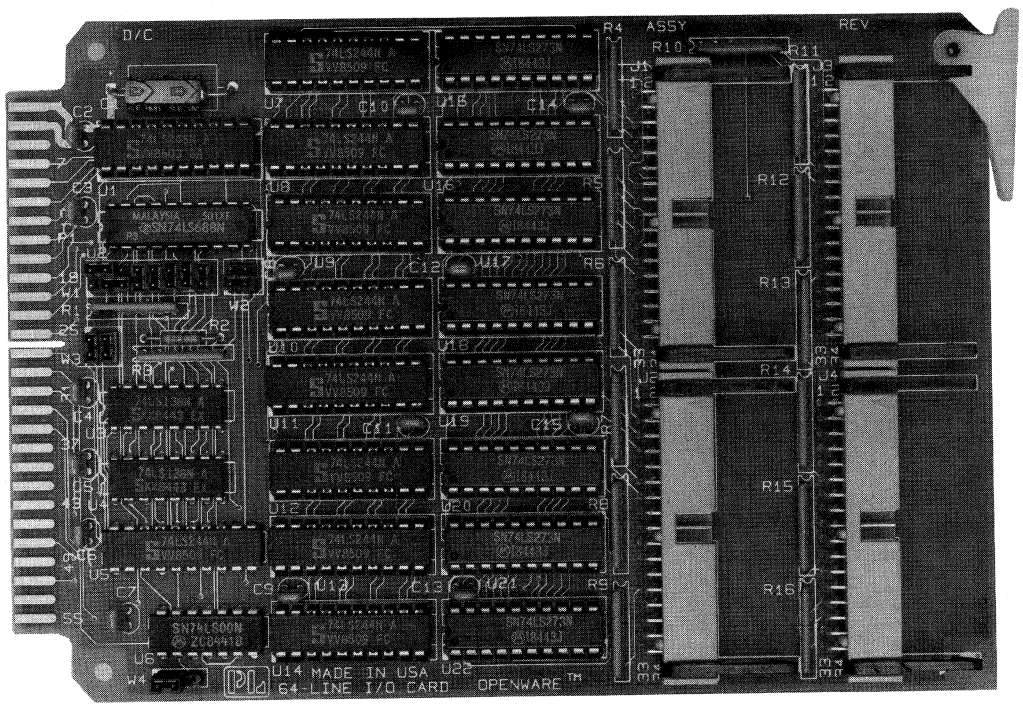


Figure 1-1. 7614 TTL Input/Output Card

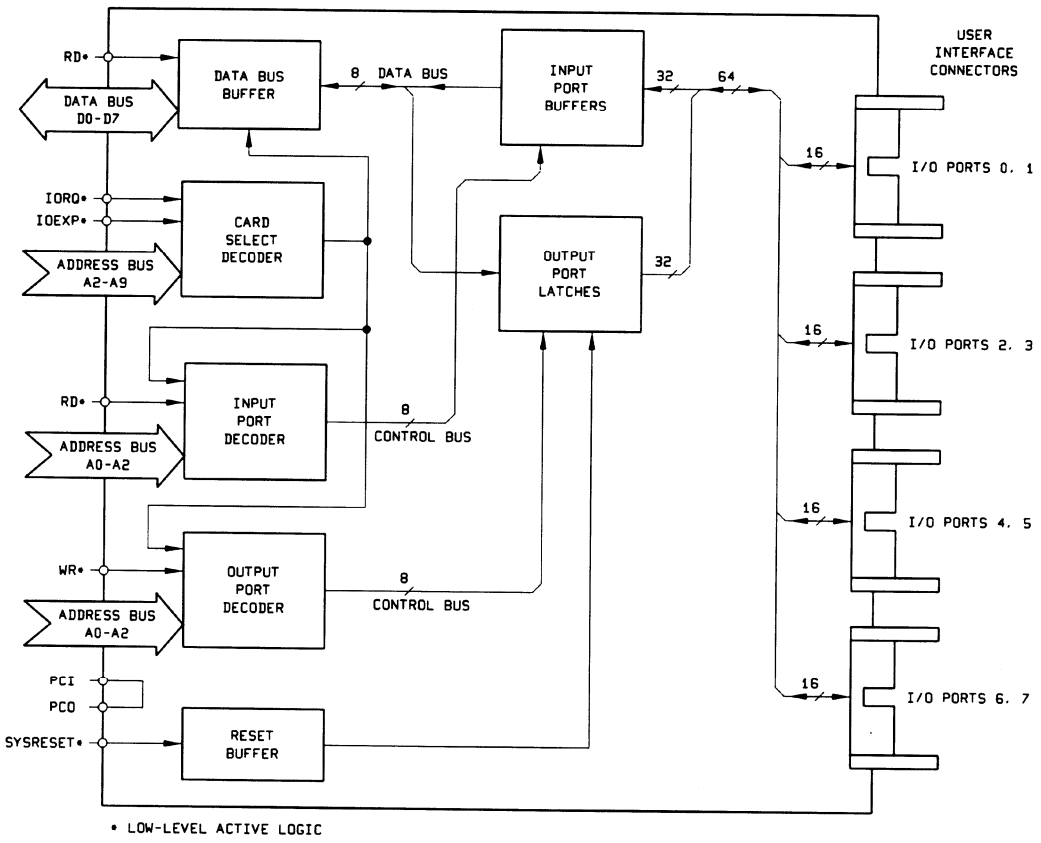


Figure 1-2. Block Diagram

FUNCTIONAL DESCRIPTION

The functional description defines each block in the 7614 block diagram shown in Figure 1-2. The block diagram and functional description are designed to familiarize the user with terms used throughout this manual.

Data Bus Buffer

The Data Bus Buffer provides buffering and direction control for the STD BUS signals D0-D7. The Data Bus Buffer 3-states when the 7614 is not selected.

Card Select Decoder

The Card Select Decoder monitors I/O Request (IORQ*), I/O expansion (IEOXP), and up to 10 address lines (A0-A9) to determine if the 7614 is selected. In systems with an 8-bit I/O address bus (e.g., 8085, Z80), the 7614 decodes all 8 address lines for up to 64 cards. In systems with a 16-bit I/O address bus (e.g., 8088), the 7614 decodes the lower 10 address lines for up to 256 cards.

Port Decoders

The Port Decoders utilize address lines A0-A2 and either read (RD*) or Write (WR*) to select one of the input or output ports on the 7614. The 7614 card has eight ports that can be individually configured as input, output, or output with readback. These configurations make it possible for the 7614 to perform all functions possible with the Pro-Log 7602A, 7603A, and 7604A TTL I/O cards. The 7614 card also operates as four bidirectional ports using four consecutive port addresses (7601A).

Input Port Buffers

The Input Port Buffers provide signal buffering between the user interface connectors and the data buffer. The input lines are connected so the current status of a given output port can be read by the corresponding input (readback). If the output latch for a given port is removed, the port can be used as an input port.

Output Port Latches

The Output Port Latches hold the data present during the last decoded write cycle. The latches are cleared with power-on reset (SYSRESET*). The data present at the output of the port latches is not inverted.

User Interface Connectors

The User Interface Connectors are 34-pin, right-angle, latching headers. Two I/O ports (16 lines) are available at each connector. Alternating signal and ground lines at each connector help to reduce signal interaction and increase electromagnetic noise immunity.

SPECIFICATIONS

The 7614 decodes up to 10 bits of I/O address for systems with a 16-bit address bus (e.g., 8088). The upper two bits can be jumper disabled for an 8-bit address bus (e.g., 8085, Z80).

General Specifications

I/O Mapping: The as-shipped I/O port address of the 7614 is 00-07 hex. Address lines A0-A7 are decoded and the card is enabled with the I/O expansion line (IOEXP) low. Address lines A8 and A9 are jumpered for a "don't care" condition.

Input Buffers and Output Latches: All input and output devices are socketed.

Mode: As shipped, the 7614 card is configured as having eight output ports with readback.

Electrical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Specified)

- Supply Voltage, Vcc: 0 to 7V
- Operating Free-Air Temperature Range: 0 to +65°C
- Storage Temperature Range: -40°C to +75°C
- Noncondensing Relative Humidity: 5% to 95%

OPERATING CONDITIONS	MIN	TYP.	MAX	UNIT
Supply Voltage, Vcc	4.75	5.00	5.25	V

Electrical Characteristics Over Operating Free-Air Temperature Range (Unless Otherwise Specified)

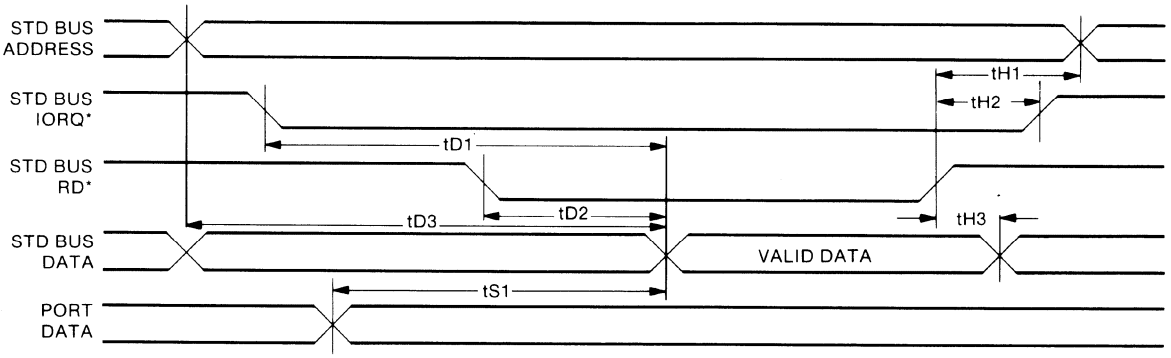
PARAMETER	MIN	TYP.	MAX	UNIT
Supply Current, Icc	—	550[1]	910	mA
Mean Time Between Failures, MTBF[2]		35		card yr/failure[3]
User Interface Input Hysteresis	0.2	0.4		V

[1]Subtract 32 mA maximum for each input buffer (LS244) removed and 17 mA maximum for each output latch (LS273) removed.

[2]MTBF calculations are based on component standard failure rates specified in *Failure Rates and MTBF*, document #111443, revision C.

[3]Card year/failure is the average time, in years, before the card will fail.

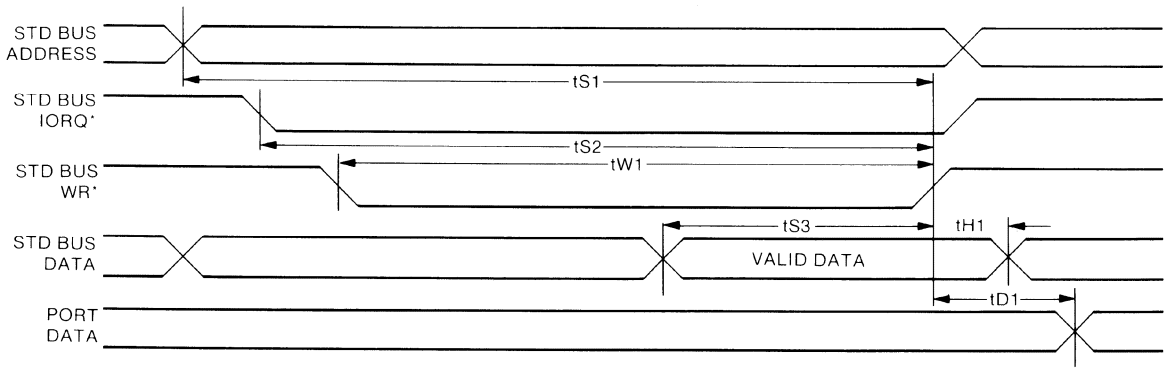
All logic signal levels related the 7614 that appear on the STD BUS conform to the STD BUS TTL requirements as specified in the general *STD Series 7000 and 7C00 Specification,* document #111684, revision B.



SYMBOL	PARAMETER	MIN	MAX
tD1	Data delay from IORQ* active		150
tD2	Data delay from RD* active		110
tD2[1]	Data delay from address valid		130
tH1	Address hold after RD* inactive	30	
tH2	IORQ* hold after RD* inactive	50	
tH3	Data hold after RD* inactive	15	
tS1	Port data setup before STD data valid	40	

[1]tD2 is equivalent to t_{AR} in the *STD BUS Specification and Practice*
All times given in nanoseconds

Figure 1-3. Read Timing



SYMBOL	PARAMETER	MIN	MAX
tD1	Port delay from WR* inactive		80
tH1[1]	Data hold after WR* inactive	55	
tS1	Address setup before WR* inactive	100	
tS2	IORQ* setup before WR* inactive	110	
tS3[2]	Data setup before WR* inactive	30	
tW1	WR* pulse width	75	

[1]tH1 is equivalent to t_{HWD} in the *STD BUS Specification and Practice*
[2]tS3 is equivalent to t_{SWD} in the *STD BUS Specification and Practice*
All times given in nanoseconds

Figure 1-4. Write Timing

Mechanical Specifications

The 7614 meets all general mechanical specifications of the STD BUS Series 7000 as given in the General STD Series 7000 and 70C00 Specification, document #111684, revision B.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2			+5V	1			+5V
4			GROUND	3			GROUND
6			DCPWRDWN*	5			VBATT
8	1	55	D7	7	55	1	D3
10	1	55	D6	9	55	1	D2
12	1	55	D5	11	55	1	D1
14	1	55	D4	13	55	1	D0
16			A15	15		1	A7
18			A14	17		1	A6
20			A13	19		1	A5
22			A12	21		1	A4
24			A11	23		1	A3
26			A10	25		1	A2
28	1		A9	27		1	A1
30	1		A8	29		1	A0
32	1		RD*	31		1	WR*
34			MEMRQ*	33		1	IORQ*
36			MEMEX	35		1	IOEXP
38			MCSYNC*	37			REFRESH*
40			STATUS 0*	39			STATUS 1*
42			BUSRQ*	41			BUSAK*
44			INTRQ*	43			INTAK*
46			NMIRQ*	45			WAITRQ*
48			PBRESET*	47		1	SYSRESET*
50			CNTRL*	49			CLOCK*
52	IN		PCI	51	OUT		PCO
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

* Low-level active logic

One LSTTL load = -0.4 mA

Figure 1-5. STD Edge Connector

User Interface

The input and output port data of the 7614 card is accessed at four latching header connectors. The pinout of these connectors is shown in Figures 1-6 through 1-9 on the following pages.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
GROUND	OUT	2		1	16	4	4-0
GROUND	OUT	4		3	16	4	4-1
GROUND	OUT	6		5	16	4	4-2
GROUND	OUT	8		7	16	4	I/O Port 4 4-3
GROUND	OUT	10		9	16	4	4-4
GROUND	OUT	12		11	16	4	4-5
GROUND	OUT	14		13	16	4	4-6
GROUND	OUT	16		15	16	4	4-7
GROUND	OUT	18		17	16	4	5-0
GROUND	OUT	20		19	16	4	5-1
GROUND	OUT	22		21	16	4	5-2
GROUND	OUT	24		23	16	4	5-3
GROUND	OUT	26		25	16	4	I/O Port 5 5-4
GROUND	OUT	28		27	16	4	5-5
GROUND	OUT	30		29	16	4	5-6
GROUND	OUT	32		31	16	4	5-7
GROUND	OUT	34		33	OUT		GROUND

* Low-level active logic
1 LSTTL load = -0.4 mA

Figure 1-6. User Interface Connector J1

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
GROUND	OUT	2		1	16	4	6-0
GROUND	OUT	4		3	16	4	6-1
GROUND	OUT	6		5	16	4	6-2
GROUND	OUT	8		7	16	4	I/O Port 6 6-3
GROUND	OUT	10		9	16	4	6-4
GROUND	OUT	12		11	16	4	6-5
GROUND	OUT	14		13	16	4	6-6
GROUND	OUT	16		15	16	4	6-7
GROUND	OUT	18		17	16	4	7-0
GROUND	OUT	20		19	16	4	7-1
GROUND	OUT	22		21	16	4	7-2
GROUND	OUT	24		23	16	4	7-3
GROUND	OUT	26		25	16	4	I/O Port 7 7-4
GROUND	OUT	28		27	16	4	7-5
GROUND	OUT	30		29	16	4	7-6
GROUND	OUT	32		31	16	4	7-7
GROUND	OUT	34		33	OUT		GROUND

* Low-level active logic
1 LSTTL load = -0.4 mA

Figure 1-7. User Interface Connector J2

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)							INPUT (LSTTL LOADS)
MNEMONIC							MNEMONIC
GROUND		OUT	2	1	16	4	0-0
GROUND		OUT	4	3	16	4	0-1
GROUND		OUT	6	5	16	4	0-2
GROUND		OUT	8	7	16	4	I/O Port 0 0-3
GROUND		OUT	10	9	16	4	0-4
GROUND		OUT	12	11	16	4	0-5
GROUND		OUT	14	13	16	4	0-6
GROUND		OUT	16	15	16	4	0-7
GROUND		OUT	18	17	16	4	1-0
GROUND		OUT	20	19	16	4	1-1
GROUND		OUT	22	21	16	4	1-2
GROUND		OUT	24	23	16	4	1-3
GROUND		OUT	26	25	16	4	I/O Port 1 1-4
GROUND		OUT	28	27	16	4	1-5
GROUND		OUT	30	29	16	4	1-6
GROUND		OUT	32	31	16	4	1-7
GROUND		OUT	34	33	OUT		GROUND

* Low-level active logic
1 LSTTL load = -0.4 mA

Figure 1-8. User Interface Connector J3

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)							INPUT (LSTTL LOADS)
MNEMONIC							MNEMONIC
GROUND		OUT	2	1	16	4	2-0
GROUND		OUT	4	3	16	4	2-1
GROUND		OUT	6	5	16	4	2-2
GROUND		OUT	8	7	16	4	I/O Port 2 2-3
GROUND		OUT	10	9	16	4	2-4
GROUND		OUT	12	11	16	4	2-5
GROUND		OUT	14	13	16	4	2-6
GROUND		OUT	16	15	16	4	2-7
GROUND		OUT	18	17	16	4	3-0
GROUND		OUT	20	19	16	4	3-1
GROUND		OUT	22	21	16	4	3-2
GROUND		OUT	24	23	16	4	3-3
GROUND		OUT	26	25	16	4	I/O Port 3 1-4
GROUND		OUT	28	27	16	4	3-5
GROUND		OUT	30	29	16	4	3-6
GROUND		OUT	32	31	16	4	3-7
GROUND		OUT	34	33	OUT		GROUND

* Low-level active logic
1 LSTTL load = -0.4 mA

Figure 1-9. User Interface Connector J4

Compatible mating connectors for user interface connectors J1-J4 are listed in Figure 1-10.

MANUFACTURER	CONNECTOR PART NO. WITH STRAIN RELIEF
T&B Ansley	609-3441
AMP	499506-0
SAE	P6334BRPS
3M	3414-6034

Figure 1-10. Compatible Mating Connectors

Section 2
INSTALLATION

INTRODUCTION

This section describes the procedure for installing the 7614 card into an STD BUS system. Options are included that must be considered before this card is installed.

INSTALLATION

> **CAUTION**
>
> To prevent possible damage to your STD BUS system, make sure power is off before inserting a card into the card rack or before removing a card from the rack.

The 7614 is designed to operate as part of an STD BUS system. The 7614 can be inserted into any slot in the STD BUS card rack with the ejector tab at the top as illustrated in Figure 2-1. If access to the card is needed for testing or servicing, a card extender such as the Pro-Log 7901 may be used.

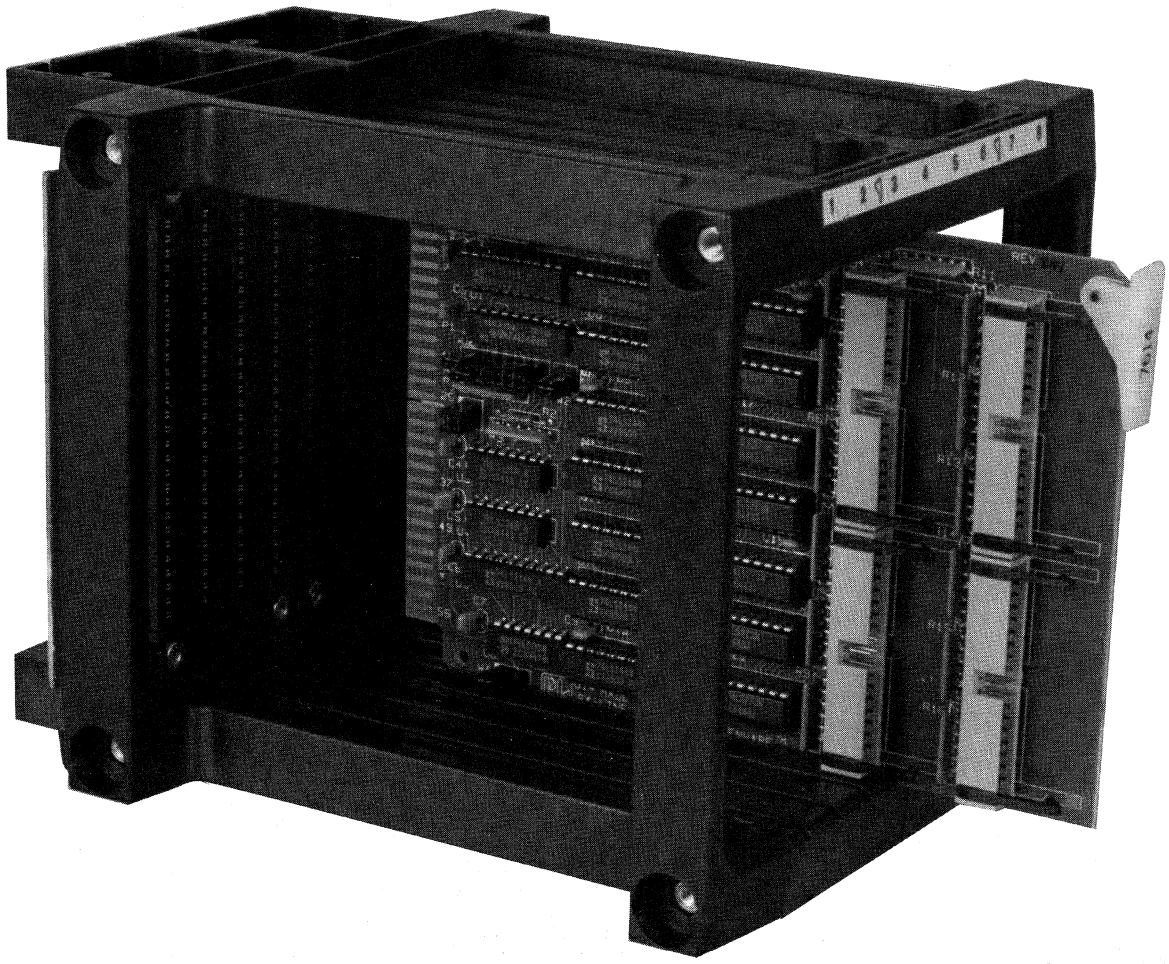
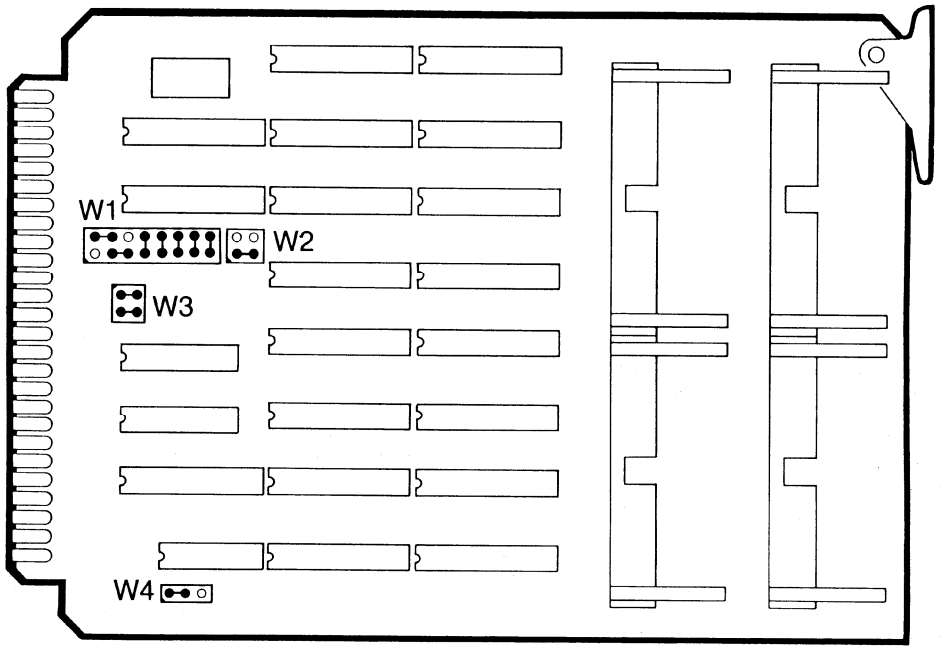


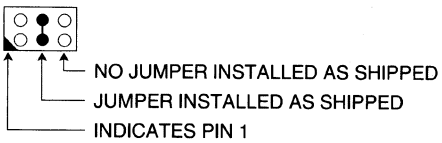
Figure 2-1. Installation

CARD LAYOUT AND JUMPERS

The 7614 has onboard slip-on jumpers to configure the card to meet system requirements. The shorting connector can be removed and installed without the use of soldering equipment.

Figure 2-2 provides a reference for the location and a brief description of each jumper on the 7614.





JUMPER GROUP	JUMPER INSTALLED	JUMPER REMOVED	DESCRIPTION	AS SHIPPED
W1			CARD SELECT DECODE • Determines the I/O port address mapping	(1)
	2-4, 3-5	—		
	7-8, 9-10	—		
	11-12, 13-14	—		
	15-16	—		
W2	1-3	2-4		
W3			PORT DECODE	
	1-2, 3-4	—	• 8 I/O port addresses (refer to Selecting a Mode, page 2-3	*
	—	1-2, 3-4	• 4 I/O port addresses (refer to Selecting a Mode, page 2-3	
W4			IOEXP DECODE	
	1-2	2-3	• Enabled with IOEXP low	*
	2-3	1-2	• Enabled with IOEXP high	
	—	1-2, 2-3	• Disregards IOEXP	

[1]Shipped at port address hex 00-07. See *I/O Mapped Card Addressing*, page 2-5 and Figure 2-5, for other configurations

Figure 2-2. Physical Layout and Jumper Options

SELECTING A MODE

The 7614 has eight ports that can be individually configured as input, output, or as output with readback. These configurations make it possible for the 7614 to perform all functions possible with the Pro-Log 7601A, 7602A, 7603A, and 7604A. These configurations are summarized in Figure 2-3.

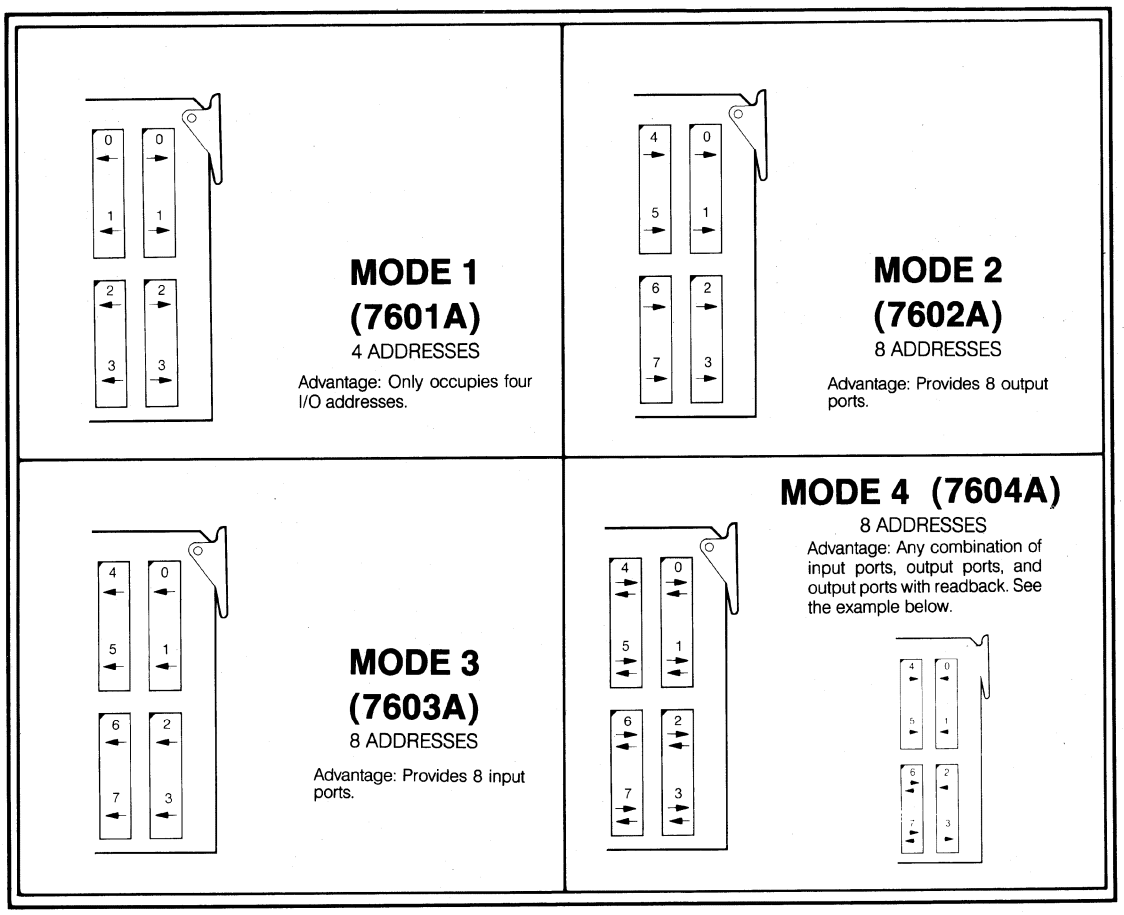


Figure 2-3. Available Functions

Refer to Figure 2-4 to configure the 7614 to the selected mode. For an input function, the output latch IC must be removed. For an output function, the input buffer IC does not need to be removed. The input ability can be ignored. In any case, each of the eight ports occupy both the input and output port functions of that address. If an IC has been removed, that function is simply inoperable.

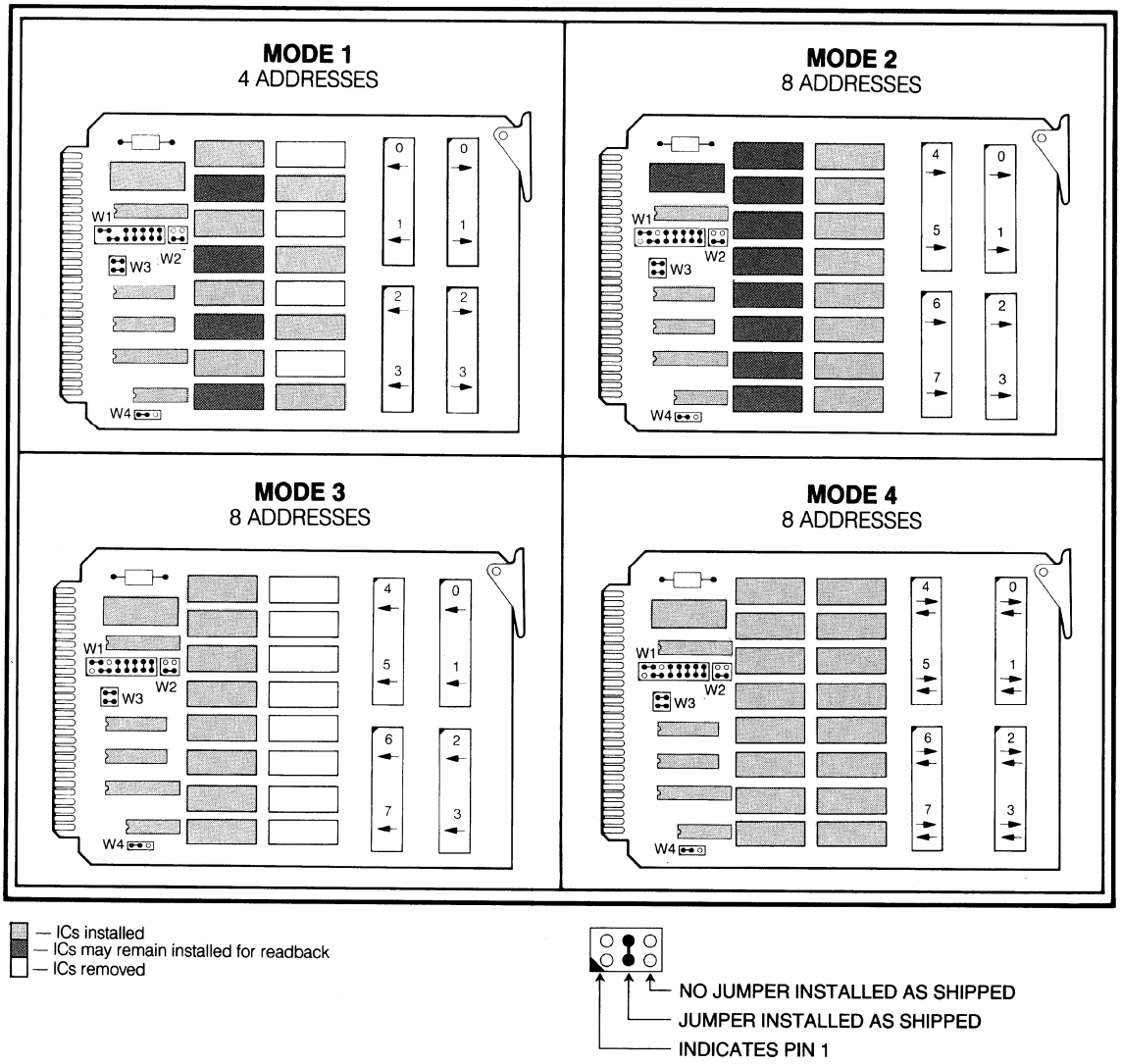


Figure 2-4. Configuring for a Function

I/O MAPPED CARD ADDRESSING

In normal operation, the 7614 is addressed directly by the processor card. The input and output ports respond to a jumper-selected combination of address lines, I/O Request (IORQ*), I/O Expansion (IOEXP) and either Read (RD*) or Write (WR*).

The 7614 occupies four or eight consecutive I/O addresses, depending upon its mapping assignment, and can be configured to decode eight or ten address lines.

EIGHT-BIT PORT ADDRESSING

The 8085 and Z80 processors provide an 8-bit I/O port address during each I/O operation. Figures 2-5 and 2-6 show W1, W2, and W3 jumper positions for 8-bit I/O port address mapping within a 16-bit address bus system. Figure 2-5 supports Mode 1 and Figure 2-6 supports Modes 2 through 4.

I/O EXPANSION

The I/O Expansion line (IOEXP) of the STD BUS allows a system to access 512 I/O ports rather than the standard 256. As shipped, the 7614 is enabled with IOEXP low (W4 1-2). Pro-Log processor cards typically connect the IOEXP line to ground. The 7614 can be enabled with IOEXP high by connecting W4 2-3. To ignore IOEXP, remove the jumper at W4.

ADDRESS RANGE	CARD SELECT DECODE HEADER									
	W1							W2	W3	
	2-4	3-5	7-8	9-10	11-12	13-14	15-16	1-2	1-2	3-4
00-03	X	X	X	X	X	X	X	X		
04-07	X	X	X	X	X	X	X			
08-0B	X	X	X	X	X	X		X		
0C-0F	X	X	X	X	X	X				
10-13	X	X	X	X	X		X	X		
14-17	X	X	X	X	X		X			
18-1B	X	X	X	X	X			X		
1C-1F	X	X	X	X	X					
20-23	X	X	X	X		X	X	X		
24-27	X	X	X	X		X	X			
28-2B	X	X	X	X		X		X		
2C-2F	X	X	X	X		X				
30-33	X	X	X	X			X	X		
34-37	X	X	X	X			X			
38-3B	X	X	X	X				X		
3C-3F	X	X	X	X						
40-43	X	X	X		X	X	X	X		
44-47	X	X	X		X	X	X			
48-4B	X	X	X		X	X		X		
4C-4F	X	X	X		X	X				
50-53	X	X	X		X		X	X		
54-57	X	X	X		X		X			
58-5B	X	X	X		X			X		
5C-5F	X	X	X		X					
60-63	X	X	X			X	X	X		
64-67	X	X	X			X	X			
68-6B	X	X	X			X		X		
6C-6F	X	X	X			X				
70-73	X	X	X				X	X		
74-77	X	X	X				X			
78-7B	X	X	X					X		
7C-7F	X	X	X							

X=Jumper installed

Figure 2-5. 8-Bit I/O Address Selection (Mode 1)

ADDRESS RANGE	CARD SELECT DECODE HEADER									
	W1							W2	W3	
	2-4	3-5	7-8	9-10	11-12	13-14	15-16	1-2	1-2	3-4
80-83	X	X		X	X	X	X	X		
84-87	X	X		X	X	X	X			
88-8B	X	X		X	X	X		X		
8C-8F	X	X		X	X	X				
90-93	X	X		X	X		X	X		
94-97	X	X		X	X		X			
98-9B	X	X		X	X			X		
9C-9F	X	X		X	X					
A0-A3	X	X		X		X	X	X		
A4-A7	X	X		X		X	X			
A8-AB	X	X		X		X		X		
AC-AF	X	X		X		X				
B0-B3	X	X		X			X	X		
B4-B7	X	X		X			X			
B8-BB	X	X		X				X		
BC-BF	X	X		X						
C0-C3	X	X			X	X	X	X		
C4-C7	X	X			X	X	X			
C8-CB	X	X			X	X		X		
CC-CF	X	X			X	X				
D0-D3	X	X			X		X	X		
D4-D7	X	X			X		X			
D8-DB	X	X			X			X		
DC-DF	X	X			X					
E0-E3	X	X				X	X	X		
E4-E7	X	X				X	X			
E8-EB	X	X				X		X		
EC-EF	X	X				X				
F0-F3	X	X					X	X		
F4-F7	X	X					X			
F8-FB	X	X						X		
FC-FF	X	X								

X=Jumper installed

Figure 2-5. (Cont'd)

ADDRESS RANGE	CARD SELECT DECODE HEADER									
	W1							W2	W3	
	2-4	3-5	7-8	9-10	11-12	13-14	15-16	1-3	1-2	3-4
00-07	X	X	X	X	X	X	X	X	X	X
08-0F	X	X	X	X	X	X		X	X	X
10-17	X	X	X	X	X		X	X	X	X
18-1F	X	X	X	X	X			X	X	X
20-27	X	X	X	X		X	X	X	X	X
28-2F	X	X	X	X		X		X	X	X
30-37	X	X	X	X			X	X	X	X
38-3F	X	X	X	X				X	X	X
40-47	X	X	X		X	X	X	X	X	X
48-4F	X	X	X		X	X		X	X	X
50-57	X	X	X		X		X	X	X	X
58-5F	X	X	X		X			X	X	X
60-67	X	X	X			X	X	X	X	X
68-6F	X	X	X			X		X	X	X
70-77	X	X	X				X	X	X	X
78-7F	X	X	X					X	X	X
80-87	X	X		X	X	X	X	X	X	X
88-8F	X	X		X	X	X		X	X	X
90-97	X	X		X	X		X	X	X	X
98-9F	X	X		X	X			X	X	X
A0-A7	X	X		X		X	X	X	X	X
A8-AF	X	X		X		X		X	X	X
B0-B7	X	X		X			X	X	X	X
B8-BF	X	X		X				X	X	X
C0-C7	X	X			X	X	X	X	X	X
C8-CF	X	X			X	X		X	X	X
D0-D7	X	X			X		X	X	X	X
D8-DF	X	X			X			X	X	X
E0-E7	X	X				X	X	X	X	X
E8-EF	X	X				X		X	X	X
F0-F7	X	X					X	X	X	X
F8-FF	X	X						X	X	X

X=Jumper installed

Figure 2-6. 8-Bit I/O Address Selection (Mode 2-4)

TEN-BIT PORT ADDRESSING

The 8088 processor (used in the IBM PC™) provides a 16-bit I/O port address during each I/O operation. Using address lines A0-A15 yields a possible 64K I/O ports. In order to utilize the I/O addressing capability of the 8088 more fully, the 7614 card offers address lines A8 and A9 for decoding. Figures 2-7 and 2-8 show the jumper positions for 10-bit I/O port address mapping within a 20-bit address bus system. Figure 2-7 supports Mode 1 and Figure 2-8 supports Modes 2 through 4.

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ADDRESS RANGE[1]	CARD SELECT DECODE HEADER										
	W1								W2	W3	
	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	1-2	1-2	3-4
0000-0003	X		X	X	X	X	X	X	X		
0004-0007	X		X	X	X	X	X	X			
0008-000B	X		X	X	X	X	X		X		
000C-000F	X		X	X	X	X	X				
0010-0013	X		X	X	X	X		X	X		
0014-0017	X		X	X	X	X		X			
0018-001B	X		X	X	X	X			X		
001C-001F	X		X	X	X	X					
0020-0023	X		X	X	X		X	X	X		
0024-0027	X		X	X	X		X	X			
0028-002B	X		X	X	X		X		X		
002C-002F	X		X	X	X		X				
0030-0033	X		X	X	X			X	X		
0034-0037	X		X	X	X			X			
0038-003B	X		X	X	X				X		
003C-003F	X		X	X	X						
0040-0043	X		X	X		X	X	X	X		
0044-0047	X		X	X		X	X	X			
0048-004B	X		X	X		X	X		X		
004C-004F	X		X	X		X	X				
0050-0053	X		X	X		X		X	X		
0054-0057	X		X	X		X		X			
0058-005B	X		X	X		X			X		
005C-005F	X		X	X		X					
0060-0063	X		X	X			X	X	X		
0064-0067	X		X	X			X	X			
0068-006B	X		X	X			X		X		
006C-006F	X		X	X			X				
0070-0073	X		X	X				X	X		
0074-0077	X		X	X				X			
0078-007B	X		X	X					X		
007C-007F	X		X	X							
0080-0083	X		X		X	X	X	X	X		
0084-0087	X		X		X	X	X	X			
0088-008B	X		X		X	X	X		X		
008C-008F	X		X		X	X	X				
0090-0093	X		X		X	X		X	X		
0094-0097	X		X		X	X		X			
0098-009B	X		X		X	X			X		
009C-009F	X		X		X	X					
00A0-00A3	X		X		X		X	X	X		
00A4-00A7	X		X		X		X	X			
00A8-00AB	X		X		X		X		X		
00AC-00AF	X		X		X		X				
00B0-00B3	X		X		X			X	X		
00B4-00B7	X		X		X			X			
00B8-00BB	X		X		X				X		
00BC-00BF	X		X		X						
00C0-00C3	X		X			X	X	X	X		
00C4-00C7	X		X			X	X	X			
00C8-00CB	X		X			X	X		X		
00CC-00CF	X		X			X	X				
00D0-00D3	X		X			X		X	X		
00D4-00D7	X		X			X		X			
00D8-00DB	X		X			X			X		
00DC-00DF	X		X			X					
00E0-00E3	X		X				X	X	X		
00E4-00E7	X		X				X	X			
00E8-00EB	X		X				X		X		
00EC-00EF	X		X				X				
00F0-00F3	X		X					X	X		
00F4-00F7	X		X					X			
00F8-00FB	X		X						X		
00FC-00FF	X		X								

X=Jumper installed
[1]Redundantly mapped for 1XXX-FXXX, X4XX, X8XX and XCXX

Figure 2-7. 10-Bit I/O Address Selection (Mode 1)

ADDRESS RANGE[1]	CARD SELECT DECODE HEADER										
	W1								W2	W3	
	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	1-2	1-2	3-4
0100-0103	X			X	X	X	X	X	X		
0104-0107	X			X	X	X	X	X			
0108-010B	X			X	X	X	X		X		
010C-010F	X			X	X	X	X				
0110-0113	X			X	X	X		X	X		
0114-0117	X			X	X	X		X			
0118-011B	X			X	X	X			X		
011C-011F	X			X	X	X					
0120-0123	X			X	X		X	X	X		
0124-0127	X			X	X		X	X			
0128-012B	X			X	X		X		X		
012C-012F	X			X	X		X				
0130-0133	X			X	X			X	X		
0134-0137	X			X	X			X			
0138-013B	X			X	X				X		
013C-013F	X			X	X						
0140-0143	X			X		X	X	X	X		
0144-0147	X			X		X	X	X			
0148-014B	X			X		X	X		X		
014C-014F	X			X		X	X				
0150-0153	X			X		X		X	X		
0154-0157	X			X		X		X			
0158-015B	X			X		X			X		
015C-015F	X			X		X					
0160-0163	X			X			X	X	X		
0164-0167	X			X			X	X			
0168-016B	X			X			X		X		
016C-016F	X			X			X				
0170-0173	X			X				X	X		
0174-0177	X			X				X			
0178-017B	X			X					X		
017C-017F	X			X							
0180-0183	X				X	X	X	X	X		
0184-0187	X				X	X	X	X			
0188-018B	X				X	X	X		X		
018C-018F	X				X	X	X				
0190-0193	X				X	X		X	X		
0194-0197	X				X	X		X			
0198-019B	X				X	X			X		
019C-019F	X				X	X					
01A0-01A3	X				X		X	X	X		
01A4-01A7	X				X		X	X			
01A8-01AB	X				X		X		X		
01AC-01AF	X				X		X				
01B0-01B3	X				X			X	X		
01B4-01B7	X				X			X			
01B8-01BB	X				X				X		
01BC-01BF	X				X						
01C0-01C3	X					X	X	X	X		
01C4-01C7	X					X	X	X			
01C8-01CB	X					X	X		X		
01CC-01CF	X					X	X				
01D0-01D3	X					X		X	X		
01D4-01D7	X					X		X			
01D8-01DB	X					X			X		
01DC-01DF	X					X					
01E0-01E3	X						X	X	X		
01E4-01E7	X						X	X			
01E8-01EB	X						X		X		
01EC-01EF	X						X				
01F0-01F3	X							X	X		
01F4-01F7	X							X			
01F8-01FB	X								X		
01FC-01FF	X										

X=Jumper Installed
[1]Redundantly mapped for 1XXX-FXXX, X4XX, X8XX and XCXX

Figure 2-7. (Con't)

ADDRESS RANGE[1]	CARD SELECT DECODE HEADER										
	W1								W2	W3	
	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	1-2	1-2	3-4
0200-0203			X	X	X	X	X	X	X		
0204-0207			X	X	X	X	X	X			
0208-020B			X	X	X	X	X		X		
020C-020F			X	X	X	X	X				
0210-0213			X	X	X	X		X	X		
0214-0217			X	X	X	X		X			
0218-021B			X	X	X	X			X		
021C-021F			X	X	X	X					
0220-0223			X	X	X		X	X	X		
0224-0227			X	X	X		X	X			
0228-022B			X	X	X		X		X		
022C-022F			X	X	X		X				
0230-0233			X	X	X			X	X		
0234-0237			X	X	X			X			
0238-023B			X	X	X				X		
023C-023F			X	X	X						
0240-0243			X	X		X	X	X	X		
0244-0247			X	X		X	X	X			
0248-024B			X	X		X	X		X		
024C-024F			X	X		X	X				
0250-0253			X	X		X		X	X		
0254-0257			X	X		X		X			
0258-025B			X	X		X			X		
025C-025F			X	X		X					
0260-0263			X	X			X	X	X		
0264-0267			X	X			X	X			
0268-026B			X	X			X		X		
026C-026F			X	X			X				
0270-0273			X	X				X	X		
0274-0277			X	X				X			
0278-027B			X	X					X		
027C-027F			X	X							
0280-0283			X		X	X	X	X	X		
0284-0287			X		X	X	X	X			
0288-028B			X		X	X	X		X		
028C-028F			X		X	X	X				
0290-0293			X		X	X		X	X		
0294-0297			X		X	X		X			
0298-029B			X		X	X			X		
029C-029F			X		X	X					
02A0-02A3			X		X		X	X	X		
02A4-02A7			X		X		X	X			
02A8-02AB			X		X		X		X		
02AC-02AF			X		X		X				
02B0-02B3			X		X			X	X		
02B4-02B7			X		X			X			
02B8-02BB			X		X				X		
02BC-02BF			X		X						
02C0-02C3			X			X	X	X	X		
02C4-02C7			X			X	X	X			
02C8-02CB			X			X	X		X		
02CC-02CF			X			X	X				
02D0-02D3			X			X		X	X		
02D4-02D7			X			X		X			
02D8-02DB			X			X			X		
02DC-02DF			X			X					
02E0-02E3			X				X	X	X		
02E4-02E7			X				X	X			
02E8-02EB			X				X		X		
02EC-02EF			X				X				
02F0-02F3			X					X	X		
02F4-02F7			X					X			
02F8-02FB			X						X		
02FC-02FF			X								

X=Jumper Installed
[1]Redundantly mapped for 1XXX-FXXX, X4XX, X8XX and XCXX

Figure 2-7. (Continued)

ADDRESS RANGE[1]	CARD SELECT DECODE HEADER										
	W1								W2	W3	
	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	1-2	1-2	3-4
0300-0303				X	X	X	X	X	X		
0304-0307				X	X	X	X	X			
0308-030B				X	X	X	X		X		
030C-030F				X	X	X	X				
0310-0313				X	X	X		X	X		
0314-0317				X	X	X		X			
0318-031B				X	X	X			X		
031C-031F				X	X	X					
0320-0323				X	X		X	X	X		
0324-0327				X	X		X	X			
0328-032B				X	X		X		X		
032C-032F				X	X		X				
0330-0333				X	X			X	X		
0334-0337				X	X			X			
0338-033B				X	X				X		
033C-033F				X	X						
0340-0343				X		X	X	X	X		
0344-0347				X		X	X	X			
0348-034B				X		X	X		X		
034C-034F				X		X	X				
0350-0353				X		X		X	X		
0354-0357				X		X		X			
0358-035B				X		X			X		
035C-035F				X		X					
0360-0363				X			X	X	X		
0364-0367				X			X	X			
0368-036B				X			X		X		
036C-036F				X			X				
0370-0373				X				X	X		
0374-0377				X				X			
0378-037B				X					X		
037C-037F				X							
0380-0383					X	X	X	X	X		
0384-0387					X	X	X	X			
0388-038B					X	X	X		X		
038C-038F					X	X	X				
0390-0393					X	X		X	X		
0394-0397					X	X		X			
0398-039B					X	X			X		
039C-039F					X	X					
03A0-03A3					X		X	X	X		
03A4-03A7					X		X	X			
03A8-03AB					X		X		X		
03AC-03AF					X		X				
03B0-03B3					X			X	X		
03B4-03B7					X			X			
03B8-03BB					X				X		
03BC-03BF					X						
03C0-03C3						X	X	X	X		
03C4-03C7						X	X	X			
03C8-03CB						X	X		X		
03CC-03CF						X	X				
03D0-03D3						X		X	X		
03D4-03D7						X		X			
03D8-03DB						X			X		
03DC-03DF						X					
03E0-03E3							X	X	X		
03E4-03E7							X	X			
03E8-03EB							X		X		
03EC-03EF							X				
03F0-03F3								X	X		
03F4-03F7								X			
03F8-03FB									X		
03FC-03FF											

X=Jumper installed
[1]Redundantly mapped for 1XXX-FXXX, X4XX, X8XX and XCXX

Figure 2-7. (Continued)

ADDRESS RANGE[1]	CARD SELECT DECODE HEADER										
	W1								W2	W3	
	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	1-3	1-2	3-4
0000-0007	X		X	X	X	X	X	X	X	X	X
0008-000F	X		X	X	X	X	X		X	X	X
0010-0017	X		X	X	X	X		X	X	X	X
0018-001F	X		X	X	X	X			X	X	X
0020-0027	X		X	X	X		X	X	X	X	X
0028-002F	X		X	X	X		X		X	X	X
0030-0037	X		X	X	X			X	X	X	X
0038-003F	X		X	X	X				X	X	X
0040-0047	X		X	X		X	X	X	X	X	X
0048-004F	X		X	X		X	X		X	X	X
0050-0057	X		X	X		X		X	X	X	X
0058-005F	X		X	X		X			X	X	X
0060-0067	X		X	X			X	X	X	X	X
0068-006F	X		X	X			X		X	X	X
0070-0077	X		X	X				X	X	X	X
0078-007F	X		X	X					X	X	X
0080-0087	X		X		X	X	X	X	X	X	X
0088-008F	X		X		X	X	X		X	X	X
0090-0097	X		X		X	X		X	X	X	X
0098-009F	X		X		X	X			X	X	X
00A0-00A7	X		X		X		X	X	X	X	X
00A8-00AF	X		X		X		X		X	X	X
00B0-00B7	X		X		X			X	X	X	X
00B8-00BF	X		X		X				X	X	X
00C0-00C7	X		X			X	X	X	X	X	X
00C8-00CF	X		X			X	X		X	X	X
00D0-00D7	X		X			X		X	X	X	X
00D8-00DF	X		X			X			X	X	X
00E0-00E7	X		X				X	X	X	X	X
00E8-00EF	X		X				X		X	X	X
00F0-00F7	X		X					X	X	X	X
00F8-00FF	X		X						X	X	X
0100-0107	X			X	X	X	X	X	X	X	X
0108-010F	X			X	X	X	X		X	X	X
0110-0117	X			X	X	X		X	X	X	X
0118-011F	X			X	X	X			X	X	X
0120-0127	X			X	X		X	X	X	X	X
0128-012F	X			X	X		X		X	X	X
0130-0137	X			X	X			X	X	X	X
0138-013F	X			X	X				X	X	X
0140-0147	X			X		X	X	X	X	X	X
0148-014F	X			X		X	X		X	X	X
0150-0157	X			X		X		X	X	X	X
0158-015F	X			X		X			X	X	X
0160-0167	X			X			X	X	X	X	X
0168-016F	X			X			X		X	X	X
0170-0177	X			X				X	X	X	X
0178-017F	X			X					X	X	X
0180-0187	X				X	X	X	X	X	X	X
0188-018F	X				X	X	X		X	X	X
0190-0197	X				X	X		X	X	X	X
0198-019F	X				X	X			X	X	X
01A0-01A7	X				X		X	X	X	X	X
01A8-01AF	X				X		X		X	X	X
01B0-01B7	X				X			X	X	X	X
01B8-01BF	X				X				X	X	X
01C0-01C7	X					X	X	X	X	X	X
01C8-01CF	X					X	X		X	X	X
01D0-01D7	X					X		X	X	X	X
01D8-01DF	X					X			X	X	X
01E0-01E7	X						X	X	X	X	X
01E8-01EF	X						X		X	X	X
01F0-01F7	X							X	X	X	X
01F8-01FF	X								X	X	X

X=Jumper installed
[1]Redundantly mapped for 1XXX-FXXX, X4XX, X8XX and XCXX

Figure 2-8. 10-Bit I/O Address Selection (Mode 2-4)

ADDRESS RANGE[1]	CARD SELECT DECODE HEADER										
	W1								W2	W3	
	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	1-3	1-2	3-4
0200-0207			X	X	X	X	X	X	X	X	X
0208-020F			X	X	X	X	X		X	X	X
0210-0217			X	X	X	X		X	X	X	X
0218-021F			X	X	X	X			X	X	X
0220-0227			X	X	X		X	X	X	X	X
0228-022F			X	X	X		X		X	X	X
0230-0237			X	X	X			X	X	X	X
0238-023F			X	X	X				X	X	X
0240-0247			X	X		X	X	X	X	X	X
0248-024F			X	X		X	X		X	X	X
0250-0257			X	X		X		X	X	X	X
0258-025F			X	X		X			X	X	X
0260-0267			X	X			X	X	X	X	X
0268-026F			X	X			X		X	X	X
0270-0277			X	X				X	X	X	X
0278-027F			X	X					X	X	X
0280-0287			X		X	X	X	X	X	X	X
0288-028F			X		X	X	X		X	X	X
0290-0297			X		X	X		X	X	X	X
0298-029F			X		X	X			X	X	X
02A0-02A7			X		X		X	X	X	X	X
02A8-02AF			X		X		X		X	X	X
02B0-02B7					X			X	X	X	X
02B8-02BF			X		X				X	X	X
02C0-02C7			X			X	X	X	X	X	X
02C8-02CF			X			X	X		X	X	X
02D0-02D7			X			X		X	X	X	X
02D8-02DF			X			X			X	X	X
02E0-02E7			X				X	X	X	X	X
02E8-02EF			X				X		X	X	X
02F0-02F7			X					X	X	X	X
02F8-02FF			X						X	X	X
0300-0307				X	X	X	X	X	X	X	X
0308-030F				X	X	X	X		X	X	X
0310-0317				X	X	X		X	X	X	X
0318-031F				X	X	X			X	X	X
0320-0327				X	X		X	X	X	X	X
0328-032F				X	X		X		X	X	X
0330-0337				X	X			X	X	X	X
0338-033F				X	X				X	X	X
0340-0347				X		X	X	X	X	X	X
0348-034F				X		X	X		X	X	X
0350-0357				X		X		X	X	X	X
0358-035F				X		X			X	X	X
0360-0367				X			X	X	X	X	X
0368-036F				X			X		X	X	X
0370-0377				X				X	X	X	X
0378-037F				X					X	X	X
0380-0387					X	X	X	X	X	X	X
0388-038F					X	X	X		X	X	X
0390-0397					X	X		X	X	X	X
0398-039F					X	X			X	X	X
03A0-03A7					X		X	X	X	X	X
03A8-03AF					X		X		X	X	X
03B0-03B7					X			X	X	X	X
03B8-03BF					X				X	X	X
03C0-03C7						X	X	X	X	X	X
03C8-03CF						X	X		X	X	X
03D0-03D7						X		X	X	X	X
03D8-03DF						X			X	X	X
03E0-03E7							X	X	X	X	X
03E8-03EF							X		X	X	X
03F0-03F7								X	X	X	X
03F8-03FF									X	X	X

X=Jumper installed
[1]Redundantly mapped for 1XXX-FXXX, X4XX, X8XX and XCXX

Figure 2-8. (Cont'd)

Section 3
OPERATION AND PROGRAMMING

OPERATION

The 7614 is an input/output port card that requires an input (RD* and IORQ*) or output (WR* and IORQ*) instruction from the host processor for data control. The data is not inverted between the STD Data Bus and the user interface connectors. Output ports with readback (Modes 2 and 4) allow the reading or verifying of the current output state. The output latches are two-state. Outputs with readback should not be used as inputs unless the associated output latch is removed.

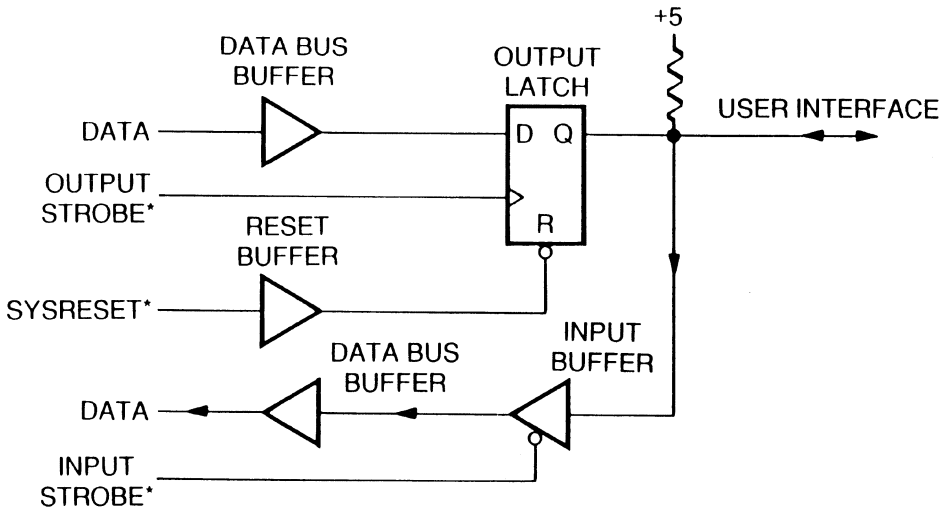

Figure 3-1. Typical 7614 I/O Circuit

Section 4
OPERATING SOFTWARE

Section 4 is normally reserved for software necessary to operate the STD card. The 7614 requires no operating software.

Section 5
MAINTENANCE

REFERENCE DRAWINGS

The schematic (Figure 5-1) and assembly drawings (Figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

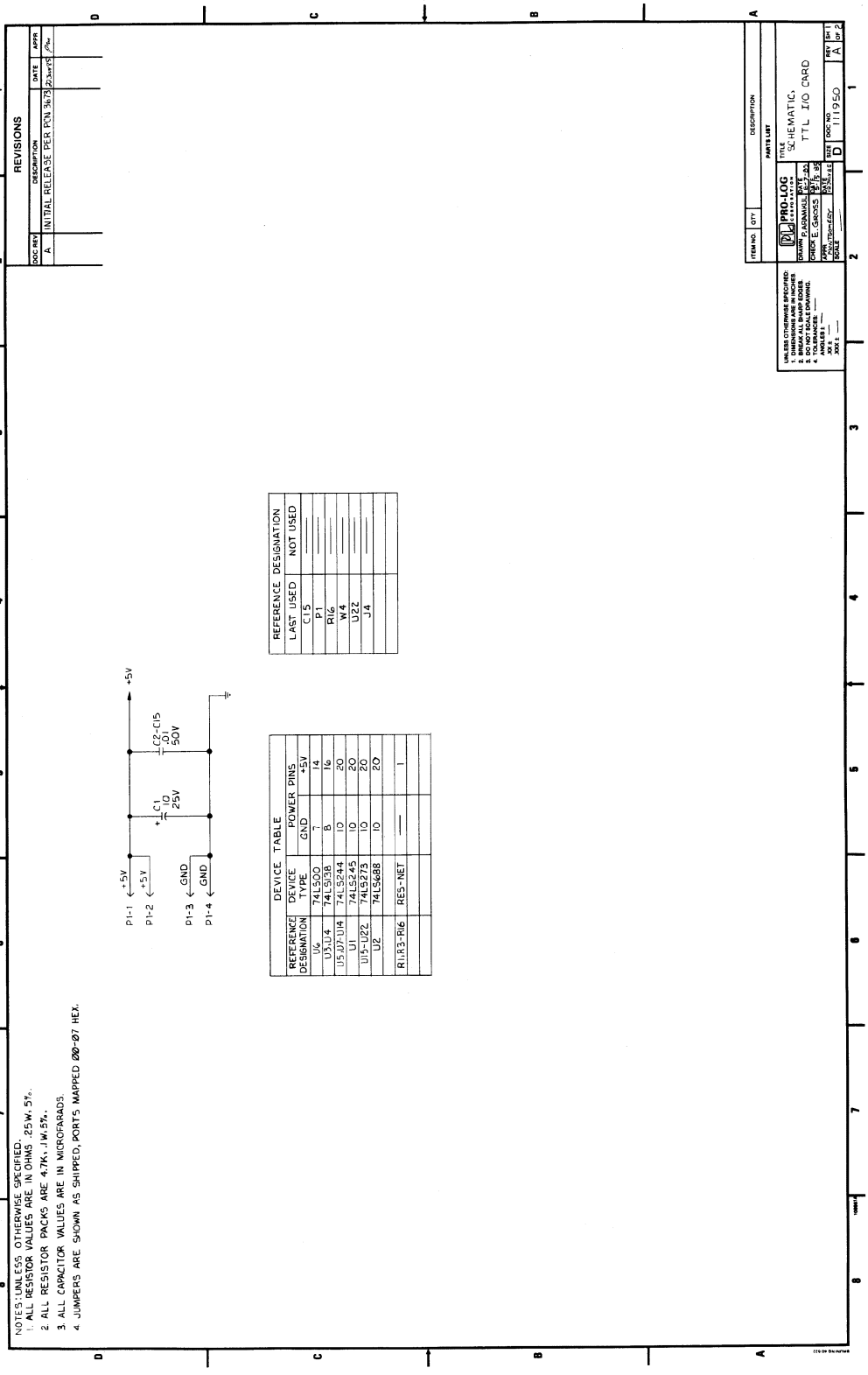

Figure 5-1. Schematic (Page 1 of 2)
FOR REFERENCE ONLY

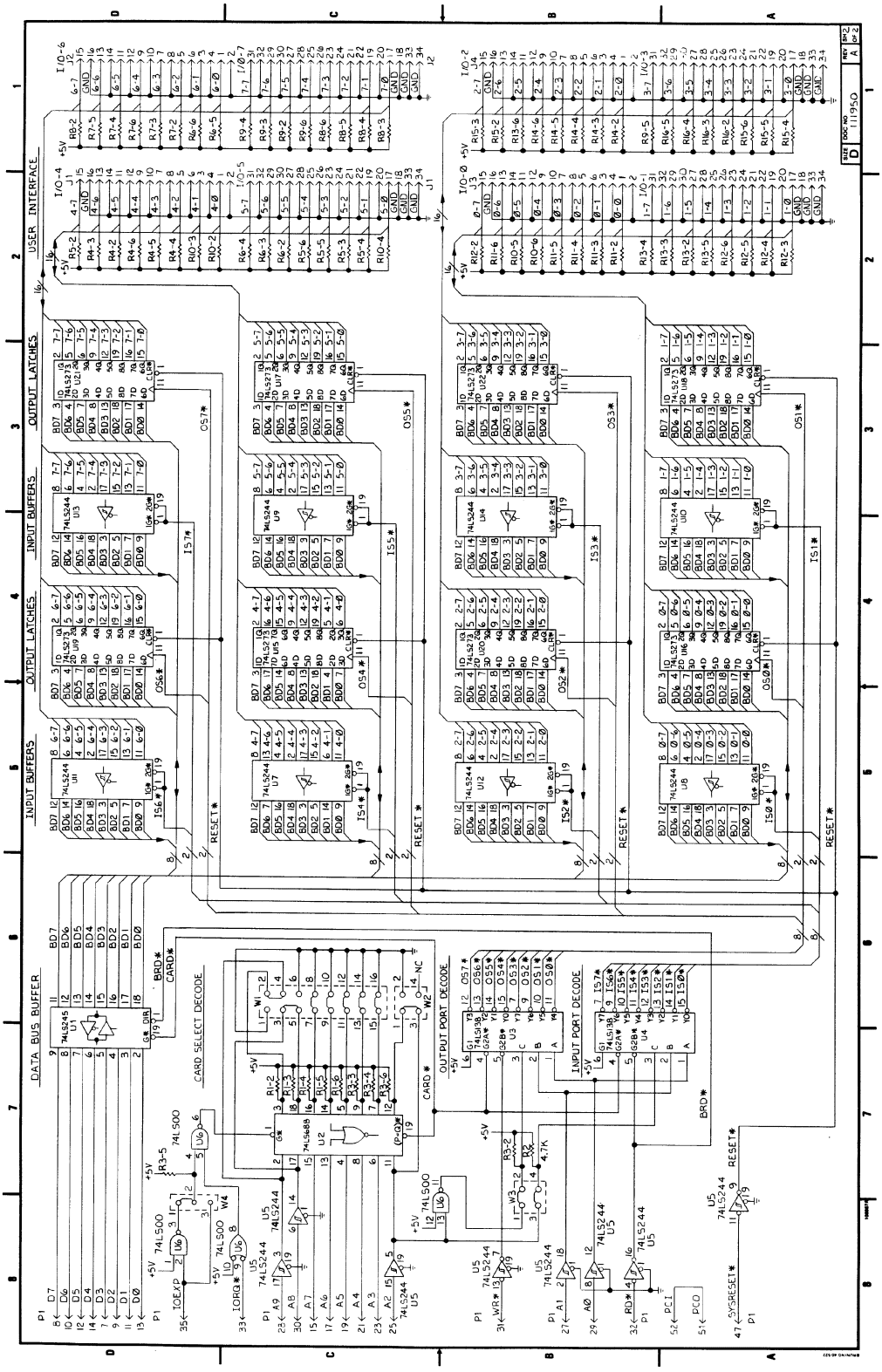

Figure 5-1. Schematic (Page 2 of 2)
FOR REFERENCE ONLY

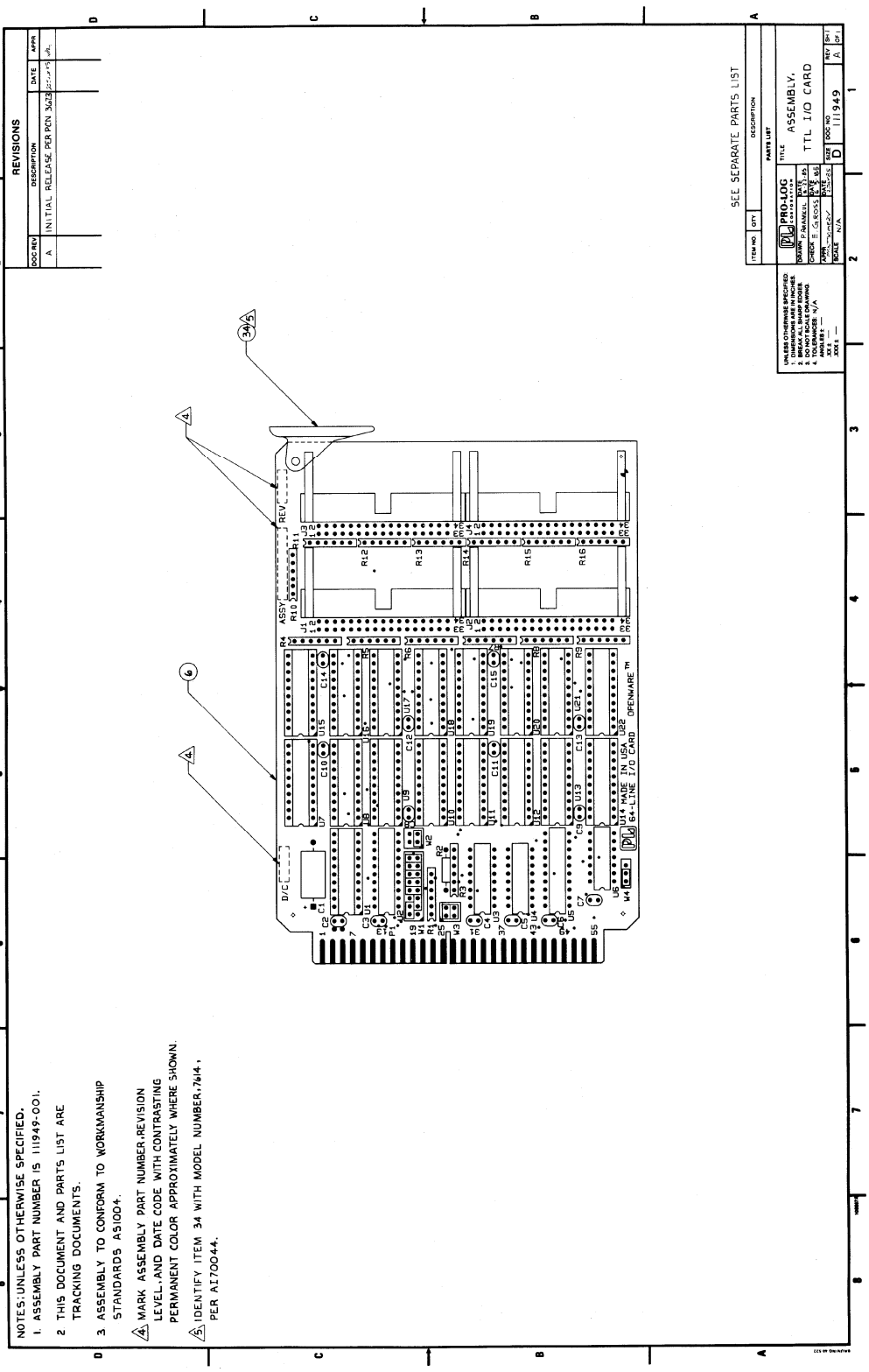

Figure 5-2. Assembly Drawing
FOR REFERENCE ONLY

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call Customer Support at (800) 538-9570, ext. 3617. In California call (408) 646-3617 from 7 a.m. to 4 p.m. (Pacific Time).
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, and reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

CAUTION

Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during handling. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2560 Garden Road
   Monterey, California 93940

   Reference CRO #_____

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment on PROM Programmers and STD BUS Series 7000 cards. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller of the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

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